ALPHA DATA

ADC-PCIE-XMC3
User Manual

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1 About the Hardware

The ADC-PCIE-XMC3 is a three quarter length PCI Express compliant XMC carrier designed to host Alpha Data ADM-XRC series of FPGA mezzanine cards.

The ADC-PCIE-XMC3 supports PCIe Gen 1 and 2 as standard. Gen 3 support is available with XMC2 connectors and compatible XMC2 modules.

Excellent fan out of XMC PN4 and P6 I/O signals to commercially available cable receptacles (SATA, Samtec TMFL, Samtec Firefly,VHDCI 68 Pin SCSI)

This carrier supports ADM-XRC series cards utilizing Virtex 6 and newer FPGAs.

The ADC-PCIE-XMC3 also supports the optional Pn4 auxiliary IO connector available on most Alpha Data mezzanine cards.

Redundant power ORing selects between the PCIe edge and the external power connector to ensure the appropriate 12V power is being applied to the XMC site.

1.1 Architecture

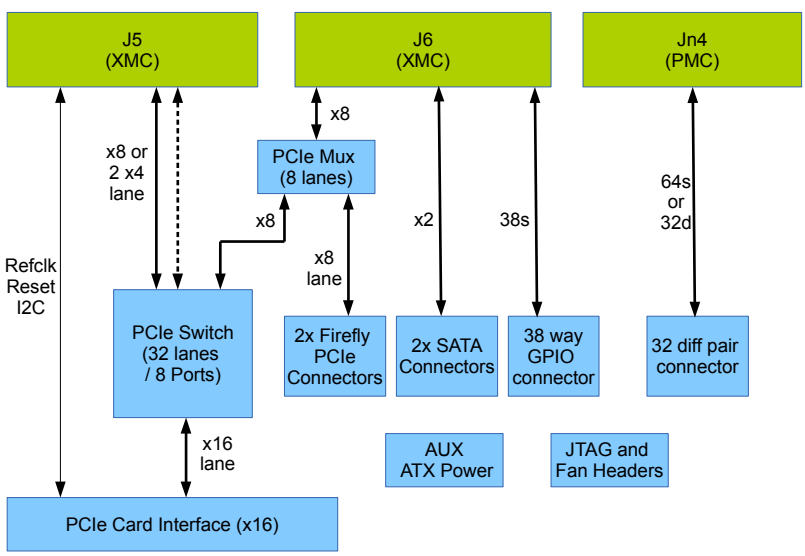

Figure 1 : ADC-PCIE-XMC3 Block Diagram

1.2 Board Features

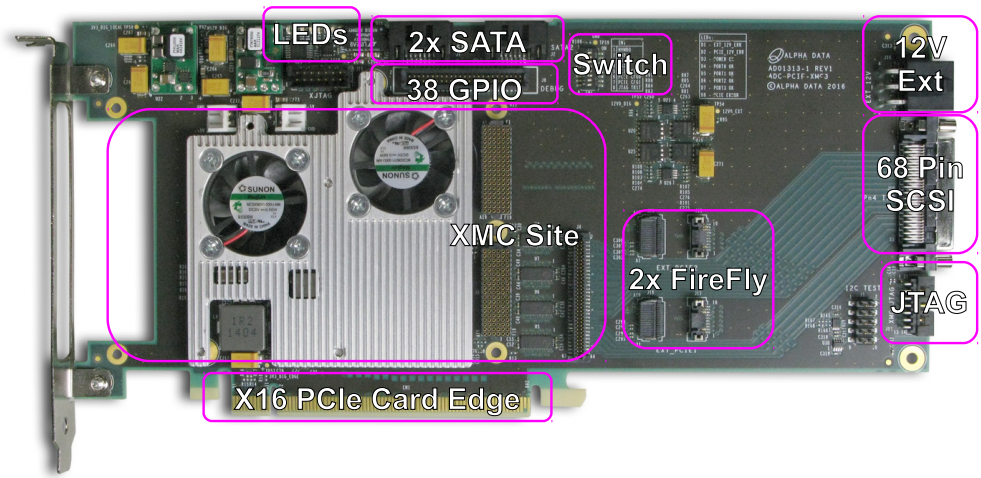

Figure 2 : Features

1.3 Limits and Measurements

The ADC-PCIE-XMC3 is a standard 3/4 length PCI express plugin card adhering to the PCI Express Card Electromechanical Specification.

Dimension	Measurement
X PCB	241.3mm
X PCB + J10 (SCSI)	246.3mm
Y	111.2mm
Z above PCB (max with XMC3)	14.47mm
Z below PCB (max with XMC3)	2.67mm
Z PCB thickness	1.57mm
Weight	182g

Table 1 : Measurements

Supply	Limit
Total Power (with XMC Card)	75W
Max Required Carrier Power (PCIe Gen3.0 @ maximum temperature 2x Firefly)	20W
Typical Required Carrier Power (PCIe Gen2.0 @ 25 degC no Firefly)	9W
VPWR (12V) to XMC site without Aux Connector	2.1A
VPWR (12V) to XMC site with AUX connector	8A
3V3 (to XMC site)	4A
M12V (to XMC site)	1A
3V3 Aux (to XMC site)	20mA

Table 2 : Power and Current Limits

Note:
The total power consumption of 75W is based on the PCIe card specification for a x16 slot.

1.4 DIP Switch (SW1)

The ADC-PCIE-XMC3 has a single 8 position DIP switch which controls the following functions. Note that a full power cycle must be performed to ensure any changes take effect.

Switch Index	Function	Off Position	On Position
1	Non-Volatile Memory Read Only	Read/Write	Read Only
2	XMC3 Address index 0	0	1
3	XMC3 Address index 1	0	1
4	XMC3 Address index 2	0	1
5	Firefly Enable	PCIe connected to XMC J6	Fireflys connected to XMC J6
6	PCIe port config (0)	see table below	see table below
7	PCIe port config (1)	see table below	see table below
8	Test Enable	Normal Operation	Test Mode

Table 3 : Switch (SW1)

Switch 7	Switch 6	J6 Port Config	J5 Port Config
OFF	OFF	invalid	invalid
ON	OFF	x8	x8
OFF	ON	x8	x4 x4
ON	ON	invalid	invalid

Table 4 : Switches 1.7 and 1.6 CFG[1:0]

1.5 LEDs

Three status LEDs display the condition of the redundant power ORing circuitry.

LED	Color	Status When Lit
D1	RED	Fault at External 12V Connector
D2	RED	Fault at PCIe Card Edge
D3	GREEN	Power OK

Table 5 : LEDs

Five status LEDs display the condition of the PCIe links.

LED	Color	Status when lit
D4	GREEN	Port 0 (PCIe Edge) link speed
D5	GREEN	Port 1 (XMC J6) link speed
D6	GREEN	Port 2 (XMC J5 - x8 or x4) link speed
D7	GREEN	Port 3 (XMC J5 - x4) link speed
D8	RED	PCIe Error has occurred

Table 6 : LEDs

The Port Status LEDs can be decoded as follows:

Flash Rate	Port Status
OFF	No Connection
1 Hz Flashing	PCIe Gen1.0
2 Hz Flashing	PCIe Gen2.0
ON	PCIe Gen3.0

Table 7 : Port Status LEDs

1.6 XMC Site

An XMC card may be fitted here with its IO area accessible externally though the rear panel.

1.7 PCIe Power Connector

This connector may be connected to the system's power supply using a standard 6-pin PCIe power cable to increase the available power to the XMC site.

1.8 Power Regulation

3.3V and -12.0V to the XMC site are generated from the +12.0V supply from the PCIe power connector or card edge.

The 3.3V power from the card edge is used to power the 2x FireFly Connectors.

1.9 Connector Descriptions

The ADC-PCIE-XMC3 is populated with a variety of connectors that help developers break out both high-speed and GPIO signals of the XMC FPGA Card.

1.9.1 XMC3 Site (Jn4, J5, J6)

The ADC-PCIE-XMC3 supports a single XMC card with an optional Pn4 connector. This XMC site is fully compliant with VITA 42.0. There are two 30mm Fans directly under the XMC site to help cool the mezzanine card.

1.9.2 SATA (J1, J2)

The ADC-PCIE-XMC3 has two standard right angle SATA receptacles for use with SATA compliant storage devices. Alpha Data offers IP to interface between Alpha Data XMC cards and mass storage devices.

1.9.3 SCSI (J12)

The ADC-PCIE-XMC3 hosts a 68 Pin industry standard SCSI connector. This interface is intended to be used for LVCMOS, LVDS, or any other electrical standard compliant with the XMC target FPGA.

This connector mates with Molex 71425-3001, VHDCI Plug Kit.

1.9.4 38 GPIO (J8)

The ADC-PCIE-XMC3 has a GPIO connector for accessing the 38 3.3V CMOS signals available from XMC site J6.

This connector is a Samtec part number TFML-125-02-L-D and has multiple mating options which can be found at www.samtec.com.

1.9.5 JTAG (J14)

A JTAG interface compatible with Xilinx a 14-pin parallel cable is available at the rear of the card. This interface can be used for debugging and standalone programming of XMC cards.

1.9.6 External 12V Power (J16)

A standard 6-pin 12V0 PCIe ATX power supply jack is available for applications which require more power than can be delivered over the PCIe Card Edge.

2 Connector Pin Assignments

2.1 Jn4 <-> J10

Signal	Jn4 Pin	J10 Pin		J10 Pin	Jn4 Pin	Signal
GND	-	1	|	35	-	GND
J4_1_P	1	2	|	18	33	J4_17_P
J4_1_N	3	36	|	52	35	J4_17_N
J4_2_P	2	3	|	19	34	J4_18_P
J4_2_N	4	37	|	53	36	J4_18_N
J4_3_P	5	4	|	20	37	J4_19_P
J4_3_N	7	38	|	54	39	J4_19_N
J4_4_P	6	5	|	21	38	J4_20_P
J4_4_N	8	39	|	55	40	J4_20_N
J4_5_P	9	6	|	22	41	J4_21_P
J4_5_N	11	40	|	56	43	J4_21_N
J4_6_P	10	7	|	23	42	J4_22_P
J4_6_N	12	41	|	57	44	J4_22_N
J4_7_P	13	8	|	24	45	J4_23_P
J4_7_N	15	42	|	58	47	J4_23_N
J4_8_P	14	9	|	25	46	J4_24_P
J4_8_N	16	43	|	59	48	J4_24_N
J4_9_P	17	10	|	26	49	J4_25_P
J4_9_N	19	44	|	60	51	J4_25_N
J4_10_P	18	11	|	27	50	J4_26_P
J4_10_N	20	45	|	61	52	J4_26_N
J4_11_P	21	12	|	28	53	J4_27_P
J4_11_N	23	46	|	62	55	J4_27_N
J4_12_P	22	13	|	29	54	J4_28_P
J4_12_N	24	47	|	63	56	J4_28_N
J4_13_P	25	14	|	30	57	J4_29_P
J4_13_N	27	48	|	64	59	J4_29_N
J4_14_P	26	15	|	31	58	J4_30_P
J4_14_N	28	49	|	65	60	J4_30_N
J4_15_P	29	16	|	32	61	J4_31_P
J4_15_N	31	50	|	66	63	J4_31_N

Table 8 : Jn4 to J10 (continued on next page)

Signal	Jn4 Pin	J10 Pin		J10 Pin	Jn4 Pin	Signal
J4_16_P	30	17	|	33	62	J4_32_P
J4_16_N	32	51	|	67	64	J4_32_N
GND	-	34	|	68	-	GND

Table 8 : Jn4 to J10

Note: All signals designated as a P/N pair are routed with 100 ohm differential tracks from supported FPGA cards to the connectors on the ADC-PCIE-XMC3

2.2 J6 <-> J1,J2

Signal	SATA Con.Pin	J6 Pin		J6 Pin	SATA Pin	Signal
J6_TX8_P	J1.2	A9	|	A19	J1.6	J6_RX8_P
J6_TX8_N	J1.3	B9	|	B19	J1.5	J6_RX8_N
J6_TX9_P	J2.2	D9	|	D19	J2.6	J6_RX9_P
J6_TX9_N	J2.3	E9	|	E19	J2.5	J6_RX9_N

Table 9 : J6 to J1,J2

2.3 J6 <-> J8

Signal	J6 Pin	J8 Pin		J8 Pin	J6 Pin	Signal
GND	-	1	|	2	-	GND
GPIO_SC_0	C1	3	|	4	C2	GPIO_SC_1
GPIO_SC_2	C3	5	|	6	C4	GPIO_SC_3
GPIO_SC_4	C5	7	|	8	C6	GPIO_SC_5
GPIO_SC_6	C7	9	|	10	C8	GPIO_SC_7
GPIO_SC_8	C9	11	|	12	C10	GPIO_SC_9
GND		13	|	14		GND
GPIO_SC_10	C11	15	|	16	C12	GPIO_SC_11
GPIO_SC_12	C13	17	|	18	C14	GPIO_SC_13
GPIO_SC_14	C15	19	|	20	C16	GPIO_SC_15
GPIO_SC_16	C17	21	|	22	C18	GPIO_SC_17
GPIO_SC_18	C19	23	|	24		NC
GND	-	25	|	26	-	GND
GPIO_SF_0	F1	27	|	28	F2	GPIO_SF_1
GPIO_SF_2	F3	29	|	30	F4	GPIO_SF_3
GPIO_SF_4	F5	31	|	32	F6	GPIO_SF_5
GPIO_SF_6	F7	33	|	34	F8	GPIO_SF_7
GPIO_SF_8	F9	35	|	36	F10	GPIO_SF_9
GND		37	|	38		GND
GPIO_SF_10	F11	39	|	40	F12	GPIO_SF_11
GPIO_SF_12	F13	41	|	42	F14	GPIO_SF_13
GPIO_SF_14	F15	43	|	44	F16	GPIO_SF_15
GPIO_SF_16	F17	45	|	46	F18	GPIO_SF_17
GPIO_SF_18	F19	47	|	48		NC
GND	-	49	|	50	-	GND

Table 10 : J6 to J8

3 Debug PCB

Each ADC-PCIE-XMC3 comes with a debug PCB that can be attached directly onto the low speed IO connector J8. Developers can solder desired connections directly to the debug PCB.

The image below shows the pin mapping from the debug PCB to the XMC3 J6 GPIO pins.

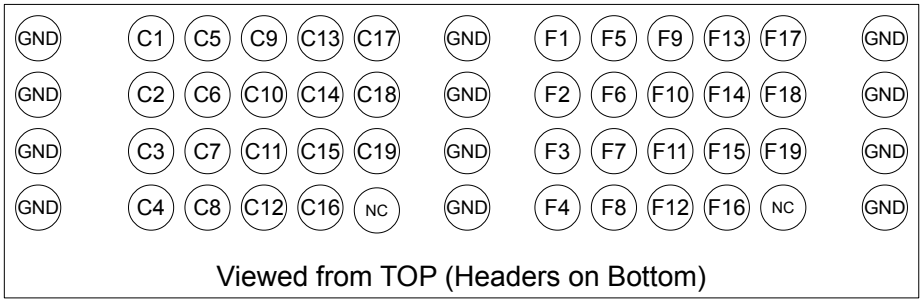

Figure 3 : Debug PCB

4 References & Specifications

ANSI/VITA 42.0	*XMC3 Standard*, December 2008, VITA, ISBN 1-885731-49-3
ANSI/VITA 42.3	*XMC3 PCI Express® Protocol Layer Standard*, June 2006, VITA, ISBN 1-885731-43-4
ANSI/IEEE 1386-2001	*IEEE Standard for a Common Mezzanine Card (CMC) Family*, October 2001, IEEE, ISBN 0-7381-2829-5

Table 11 : References

Revision History

Date	Revision	Nature of Change	ERROR
15 June 2017	0.1	Initial Draft	ERROR
18 July 2017	0.2	Fixed error in Table 4	ERROR
05 December 2017	1.0	Initial Release	ERROR
04 June 2018	1.1	Added note to power cycle after changing DIP switch settings.	ERROR

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